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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,959	10/15/2004	Fook-Luen Heng	BUR920040201US1	5958

45093 7590 01/25/2006

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EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/711,959	HENG ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *25-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/04 & 11/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication of 10/15/2004. Application 10/711,959 has been examined. In the examination of 10/711,959, claims 1-30 are pending.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-24, drawn to a method for selectively scaling an integrated circuit, classified in class 716, subclass 3.

II. Claims 25-30, drawn to a method for improving yield of an integrated circuit, classified in class 716, subclass 4.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as for selectively scaling an integrated circuit. Invention II has separate utility such as for the improvement of yield. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Richard Kotulak (Registration No. 27,712) on 01/18/2006 a provisional election was made without traverse to prosecute the invention of Group I. Affirmation of this election must be made by applicant in replying to this Office action. Claims 25-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. **Claims 1-24 are rejected under 35 U.S.C. 102(a)** as being anticipated by Regan (US Patent No. 6,756,242).

As per **claim 1**, Regan discloses a method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

defining technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

determining a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 4, line 14-26; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 3, line 15-36; col. 11, line 66-67; col. 13, line 5-13); and

in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

As per **claim 2**, Regan discloses the method of claim 1, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell (Fig. 20, #75; col. 1, line 7-16; col. 2, line 41-57; col. 7, line 7-12).

As per **claim 3**, Regan discloses the method of claim 1, wherein the placement and routing performing step includes using an optimization-based hierarchical scaling program to produce a legal layout for each problem object (col. 2, line 41-57; col. 8, line 6-11; Fig. 11; col. 8, line 41-44).

As per **claim 4**, Regan discloses the method of claim 1, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier (col. 2, line 26-40).

As per **claim 5**, Regan discloses the method of claim 1, wherein the identifying step includes:

manufacturing the design layout (col. 3, line 19-21);

testing the manufactured design layout and identifying at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

generating the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 6**, Regan discloses the method of claim 5, wherein the testing step includes characterizing operation and identifying the at least one problem object by obtaining data indicating how well objects are able to be manufactured (col. 10, line 41-53).

As per **claim 7**, Regan discloses the method of claim 5, wherein the manufacturing information generating step includes generating the scaling target for the problem object (Fig. 21, #81; col. 13, line 14-27).

As per **claim 8**, Regan discloses the method of claim 1, further comprising the step of evaluating whether a new design layout including the scaled objects achieves an expected behavior (Fig. 23; col. 14, line 34-67; Fig. 20, #75; col. 11, line 39-44).

As per **claim 9**, Regan discloses a system for selectively scaling an integrated circuit design layout (col. 10, line 27-36; col. 14, line 25-27), the system comprising the steps of:

means for identifying a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

means for defining technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

means for determining a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 4, line 14-26; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

means for determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 3, line 15-36; col. 11, line 66-67; col. 13, line 5-13); and

means for, in the case that assemble is required, performing placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

As per **claim 10**, Regan discloses the system of claim 9, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell (Fig. 20, #75; col. 1, line 7-16; col. 2, line 41-57; col. 7, line 7-12).

As per **claim 11**, Regan discloses the system of claim 9, wherein the placement and routing performing means includes means for conducting an optimization-based hierarchical scaling to produce a legal layout for each problem object (col. 2, line 41-57; col. 8, line 6-11; Fig. 11; col. 8, line 41-44).

As per **claim 12**, Regan discloses the system of claim 9, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier (col. 2, line 26-40).

As per **claim 13**, Regan discloses the system of claim 9, wherein the identifying means includes:

means for testing a manufactured design layout and identifying at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

means for generating the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 14**, Regan discloses the system of claim 13, wherein the testing means includes means for characterizing operation and identifying the at least one problem object by obtaining data indication how well objects are able to be manufactured (col. 10, line 41-53).

As per **claim 15**, Regan discloses the system of claim 13, wherein the manufacturing information generating means includes means for generating the scaling target for the problem object (Fig. 21, #81; col. 13, line 14-27).

As per **claim 16**, Regan discloses the system of claim 13, further comprising means for evaluating whether a new design layout including the scaled objects achieves an expected behavior. (Fig. 23; col. 14, line 34-67; Fig. 20, #75; col. 11, line 39-44).

As per **claim 17**, Regan discloses a computer program product comprising a computer useable medium having computer readable program code embodied therein for selectively scaling an integrated circuit design layout (col. 1, line 35-36; col. 2, line 5-6; col. 13, line 66 to col. 14, line 20), the program product comprising:

program code configured to identify a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

program code configured to define technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

program code configured to determine a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 4, line 14-26; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

program code configured to determine which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 3, line 15-36; col. 11, line 66-67; col. 13, line 5-13) ; and

program code configured to, in the case that assembly is required, perform placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

As per **claim 18**, Regan discloses the program product of claim 17, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell (Fig. 20, #75; col. 1, line 7-16; col. 2, line 41-57; col. 7, line 7-12).

As per **claim 19**, Regan discloses the program product of claim 17, wherein the placement and routing performing code includes program code configured to conduct

an optimization-based hierarchical scaling to produce a legal layout for each problem object (col. 2, line 41-57; col. 8, line 6-11; Fig. 11; col. 8, line 41-44).

As per **claim 20**, Regan discloses the program product of claim 17, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier (col. 2, line 26-40).

As per **claim 21**, Regan discloses the program product of claim 17, wherein the identifying code includes:

program code configured to test a manufactured design layout and identify at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

program code configured to generate the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 22**, Regan discloses the program product of claim 21, wherein the testing code includes program code configured to characterize operation and identify the at least one problem object by obtaining data indication how well objects are able to be manufactured (col. 10, line 41-53).

As per **claim 23**, Regan discloses the program product of claim 17, wherein the manufacturing information generating code includes program code configured to generate a scaling target for the problem object (Fig. 21, #81; col. 13, line 14-27).

As per **claim 24**, Regan discloses the program product of claim 17, further comprising program code configured to evaluate whether a new design layout including the scaled objects achieves an expected behavior (Fig. 23; col. 14, line 34-67; Fig. 20, #75; col. 11, line 39-44).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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